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M.Tech In VLSI Design. (8.56/10 CGPA ) Coursework: VLSI Design, Memory System Design, ASIC Designs, Fault-tolerant Designs, Low-Power IC Designs I Worked On FPGA Implementation Of Dynamic Memory Access Management For Multimedia Applications. The Aim Of This Project Was To Reduc Apr 12th, 2024

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In The SOPC Builder For This Project, SDRAM Is Connected As Our CPU Memory. The Clock Phase For The SDRAM Has To Be 3ns Later Than The Other Part Of The Avalon Bus. So We Used Phase Locked Loop To Generate The Clock For SDRAM. Since In Our Design, We Need To Use SRAM To St Mar 10th, 2024

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