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Min-Delay: Pulsed Latches T_t T_{cd} C_{cq} $P_w \geq - +$ hold CL Q1 D2 Q1 D2 ϕ P T P_w ϕ P
L1 ϕ P L2 T Cd T Hold T Ccq Hold Time Increased By Pulse Width 11/1/2006 VLSI
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